D2008
UHF Wireless MIC Transceiver
V2.0

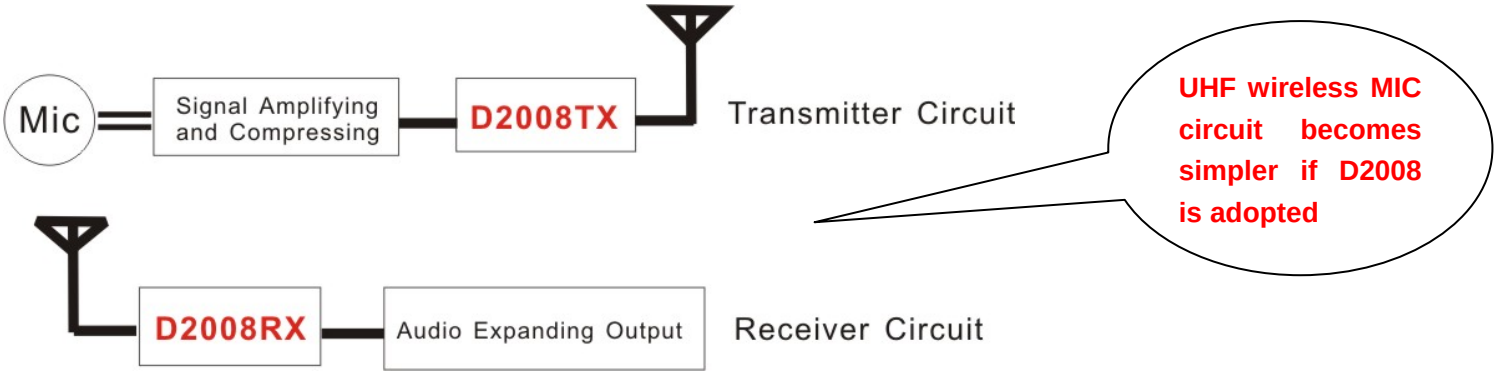
Contents

Version	Date	Remarks
V1.0	2007/12/10	The first version
V2.0	2009/07/20	RX function expanded

Add: 516 Bldg 4, National Software Park, 2 Kejizhong Rd., Shenzhen Hi-Tech Park, Shenzhen, China
Tel: （86-755）8618 5088 Fax:（86-755）8618 5000

1 Description

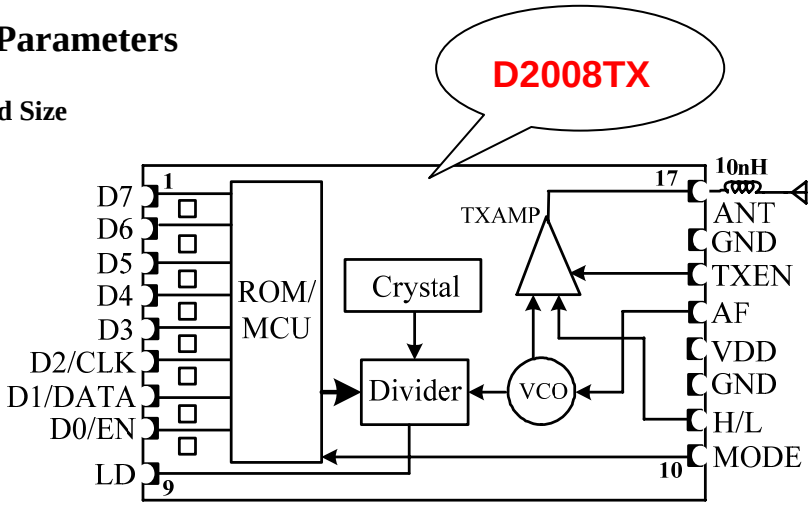
The high-frequency module is used exclusively for UHF wireless MIC. With audio circuit, transmitting module (TX) could be made into a complete wireless speaker or belt-pack transmitter. Receiving module (RX) consists of noise amplification, one time frequency mixing, twice mixing, local oscillation, MCU frequency control and other functions. With audio circuit, it could be made into a complete wireless MIC receiver. By applying D2008 directly, factories could simplify design and production of UHF wireless MIC, and adopt the module easily in mining industry and electronic consumer system equipments. RX sensitivity is -111dBm@12dBSINAD.

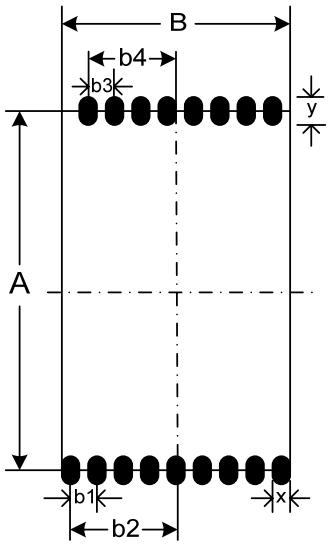


==========

2 Basic Module Parameters

2.1Pin Position and Size

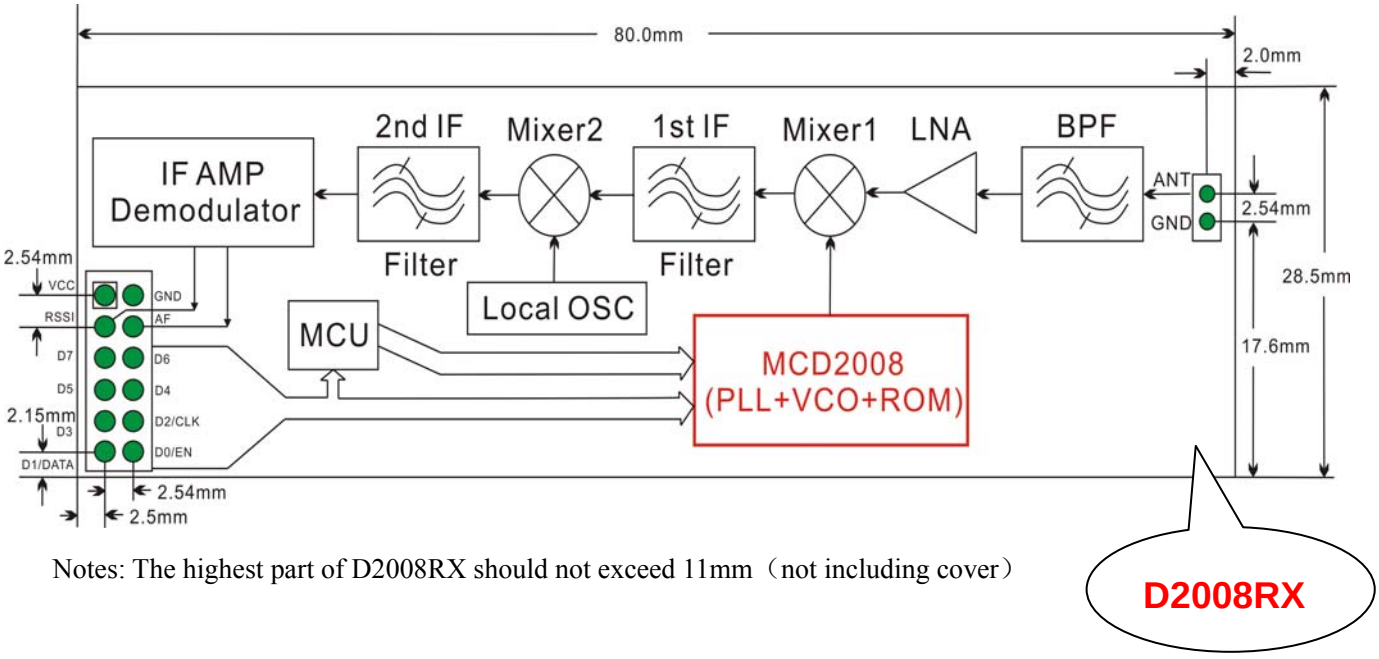




	mm
A	31.5
B	17.5
b1	2.0
b2	8.0
b3	2.0
b4	6.65
x	1.5
y	2.5

Size and welding points of

transmitting module PCB（front side）



Notes: The highest part of D2008RX should not exceed 11mm（not including cover）

2.2 Pin description

Pin No.	Type	I/O	Description
D7-D3	TX,RX	I	Input port of 8th - 4th ROM control bit. When control bit is suspended, logic level is low. When control bit is connected to VDD, logic level is high.

D2/CLK	TX,RX	I	3rd ROM control bit. CLK is clock input port of MCU serial data. On the rising edge of clock, data is input to 18-bit shift register of serial interface.
D1/DATA	TX,RX	I	2nd ROM control bit. DATA is input port of MCU serial data. The lowest bit is input first, and the last two bits are group identification codes.
D0/EN	TX,RX	I	1st ROM control bit. EN is input enable port. When EN is at high level, data in shift register would be loaded in latch distinguished by group identification codes.
GND	TX,RX	-	Ground port
VDD VCC	TX	I	Power supply input(3.9V-4.5V)。
	RX	I	Power supply input (10V~16V)。
AF	TX	I	Modulation input port. Frequency is within 30Hz-30KHz，modulation sensitivity: at 1KHz, 15mV, modulation frequency deviation is 20KHz
	RX	O	Audio demodulation output. Output range is 200±30 mV.
ANT	TX	O	Antenna output. Output impedance is 50Ω. With external antenna, ANT output port is serially connected to 10nH inductor.
	RX	I	Antenna input. Input impedance is 50Ω.
LD	TX	O	Lock detection output. When loop is locked, LD output is at high level.
MODE	TX	I	ROM and MCU mode selection bit, CMOS input. When MODE pin is at low level, module works in ROM mode. When MODE pin is at high level, module works in MCU control mode.
TXEN	TX	I	Transmitting power enable control. The amplifier is off when it is at low level. As PLL is at work, ANT output radiation power is about -56dBm. When it is at high level, ANT output rating power is 12±1dBm.
H/L	TX	I	High-low power selection pin. When H/L is at high level, ANT output power is 1±1dBm. When H/L is at low level, ANT output power is 12±1dBm.
RSSI	RX	O	Output pin of signal intensity

2.3 Recommended operating voltage and electrical property

Recommended operating voltage

Parameter		No.	Value			Unit
			The minimum value	typical value	The maximum value	
Operating voltage	D2008TX	VDD	3.9	4.0	4.5	V
	D2008RX	VCC	10		16	

Electrical property

Parameter		Test condition	Value			Unit
			The minimum value	typical value	The maximum value	
General property						
Operating frequency		Signal channel is selected within bandwidth 90MHz(restricted by filter and modulation degree)	300		1000	MHz
Number of signal channel	ROM mode	Number of signal channel within bandwidth 1.5-30MHz	1		96	
	MCU mode	Be set randomly within fixed frequency				
D0-D7 low level			-0.3		0.3	V
D0-D7 high level			0.8VDD		VDD+0.3	V
Crystal frequency				20		MHz
Lock detection				VDD		V
D2008TX						

1. RF property					
Output impedance			50		ohm
Operating current	VDD=4.0V	32	35	40	mA
Output power （ 50ohm load）	H/L=0	9	11	13	dBm
	H/L=1	-4	-1	2	
Phase noise	50Hz loop bandwidth，10KHz frequency deviation		-94		dBc/Hz
2. Audio frequency property					
Input impedance (audio input port)			10K		ohm
Transmitting frequency response	±3dB	30		30K	Hz
Modulation degree	1KHz，15mV input degree	±18	±20	±22	KHz
Ratio of SINAD	1KHz，40K modulation degree	53			dB
Ratio of signal to noise	1KHz，40K modulation degree	54			dB
Modulation distortion degree	1KHZ@±20KHz frequency deviation	1.0	1.5	2.0	%
D2008RX					
Operating current	VCC=10.0V	53	55	60	mA
Input impedance			50		ohm
Receiving sensitivity	SINAD=12dB	-118	-112	-108	dBm
Degree of audio demodulation output	20KHz modulation degree@1KHz modulation frequency	170	183	195	mV
Distortion	Signal intensity-47dBm	0.5	0.66	0.9	%
Ratio of SINAD	20KHz modulation degree	40	43	45	dB

Ratio of signal to noise	100KHz modulation degree		60		dB
RSSI output level	SINAD 30dB	1.1	1.41	1.62	V
Frequency response		30		30K	Hz

Signal channel distribution of ROM（for details please refer to *ROM Control Logic of D2008 Module*）

Frequency section	TX	RX	Number of signal channel	Space of signal channel
A	433.0MHz–437.5MHz	322.4MHz–326.9MHz	16channels	300KHz
B	790.0MHz–819.4MHz	679.4MHz–708.8MHz	16channels	200KHz-5.2MHz
C	790.3MHz–819.7MHz	679.7MHz–709.1MHz	16channels	200KHz-5.2MHz
D	726.1MHz–732.4MHz	615.5MHz–621.8MHz	16channels	300/400/500KHz
E	734.0MHz–739.1MHz	623.4MHz–628.5MHz	16channels	300/400KHz
F	739.9MHz–746.0MHz	629.3MHz–635.4MHz	16channels	300/400/500KHz
G	793.4MHz–799.1MHz	682.8MHz–688.5MHz	16channels	300/400/500KHz
H	799.6MHz–805.9MHz	689.0MHz–695.3MHz	16channels	300/400/500KHz
I	807.5MHz–812.6MHz	696.9MHz–702.0MHz	16channels	300/400/500KHz
J	813.4MHz–819.1MHz	702.8MHz–708.5MHz	16channels	300/400KHz
K	846.2MHz–851.9MHz	735.6MHz–741.3MHz	16channels	300/400/500KHz
L	854.3MHz–858.6MHz	743.7MHz–748.0MHz	16channels	200/300KHz
M	859.4MHz–864.4MHz	748.8MHz–753.8MHz	16channels	300/400/500KHz
N	840.0MHz–869.4MHz	729.4MHz–758.8MHz	16channels	200KHz-5.2MHz
O	914.2MHz–915.7MHz	903.5MHz–905.0MHz	16channels	100KHz
P	863.0MHz–864.8MHz	752.4MHz–754.2MHz	7channels	300KHz

3 Module Application

3.1 How to select different RX modules according to frequency requirement

There are three types of D2008RX module：

No.	Mode	Features
D2008RXR	ROM	With built-in frequency points of ROM in PLL chips (please download *ROM Control Logic of D2008 Module* from www.mcdevices.com.
D2008RXM	With built-in MCU	For the condition that frequency is not built-in frequency points in ROM, without external MCU. The most 256 frequency points.
D2008RXD	With external MCU	With external MCU, frequency could be changed randomly, the most 300 frequency points (restricted by 30MHz filter)

While D2008RXR module is at work, RX receiver works in ROM mode. For details please refer to 3.2.

While D2008RXM module is at work, internal MCU is used to send control word. According to users' requirement, it is within 30MHz. At most 256 frequency points could be set in 8-bit data ports, with decimal accuracy. While module is at work, logic level of D0-D7 is set according to logic table provided with module, so that frequency could be selected.

While D2008RXD module is at work, RX receiver works in MCU mode. External MCU is used to send control word. For detail please refer to 3.3 and download *D2008-2009 Programming Examples* from www.mcdevices.com.

3.2 How to use ROM mode

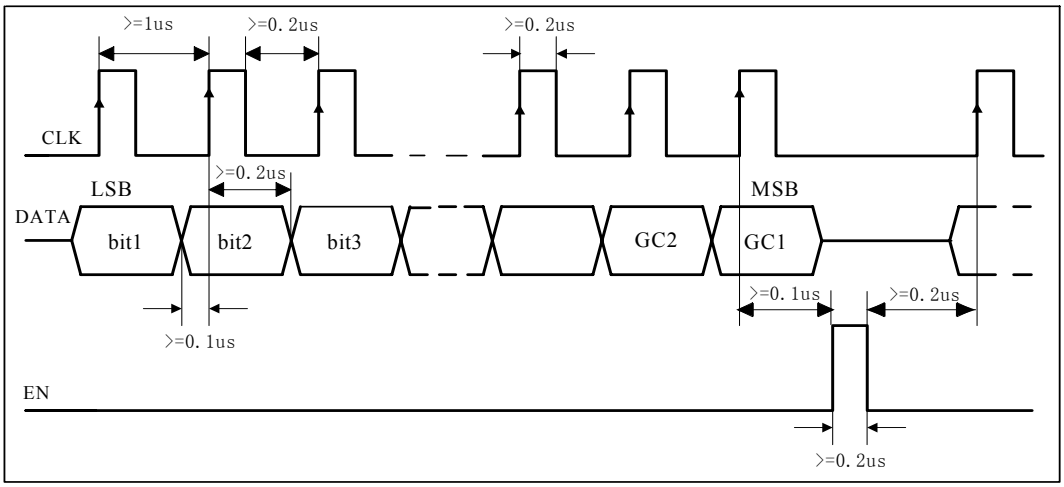
If setting TX transmitting pin MODE=0, the module works in ROM mode. And RX receiver D2008RXR only works in ROM mode. Within 300-1000MHz, 8-bit control ports (D0-D7) are used to select bandwidth 1.5-30 MHz, and then 1-96 frequency points could be made within 247 fixed frequency points. For internal ROM frequency distribution, please download *ROM Control Logic of D2008 Module* from www.mcdevices.com. By using ROM mode, programming MCU could be reduced. However, PLL could only be fixed in frequency points set by ROM.

3.3 How to set MCU mode

If setting TX transmitter MODE=1, the module works in MCU mode. RX receiver D2008RXD only works in MCU mode. In MCU mode, ports D2-CLK, D1/DATA and D0/EN are also used as input ports of serial data. Binary serial data is input from D1/DATA port, and transferred to parallel data by serial-parallel port. After it is distinguished by group identification codes, it is transmitted to reference frequency-dividing counter and channel frequency-dividing counter in turn.

All data is read into internal shift register at rising edge of CLK signal. The first configuration data to be read is LSB (the lowest bit), and the last two bits (group identification code) are used to decode the address of internal register. At rising edge of EN signal, the data in shift register is loaded in counter distinguished by group identification code.

Timing of CLK, DATA and EN signal is as follows:



Notes: (1) LSB data is input to shift register first.

(2) While it is powered on, reference frequency divider is configured first, and then channel frequency divider.

Distribution of group identification codes:

Group identification code		Controlled counter
GC1 (MSB)	GC2 (LSB)	
1	0	channel frequency-dividing counter
1	1	reference frequency-dividing counter

3.4 How to configure programmable counter

3.4.1 Reference frequency-dividing counter R

Reference frequency-dividing counter provides reference frequency for PLL, with number of frequency-dividing 10. The total frequency-dividing range is 6～2046.

LSB configuration word MSB

R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	GC2=1	GC1=1

3.4.2 Channel frequency-dividing counter N

The programmable frequency-dividing counter consists of a 4-bit SWALLOW counter and a 12-bit PULSE counter. And the frequency-dividing range made by the frequency divider and 64/68 prescaler is 192～262140.

LSB configuration word MSB

N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	GC2=0	GC1=1

|--------swallow counter----------|----------pulse counter----------|group identification code

3.4.3 Configuration example

Example 1：Reference frequency 25 KHz is made from 20MHz crystal.

- Total number of frequency division 2R = 20MHz÷25KHz = 800
- Programmable number of frequency division R = 800÷2 = 400
- Binary (10bit) R=0110010000
- Group identification code of reference frequency divider "11"
- Configuration word (12bit) "110110010000"

LSB (input to register first) → MSB

0	0	0	0	1	0	0	1	1	0	1	1

Example 2：VCO frequency 863MHz is generated from reference frequency 25 KHz.

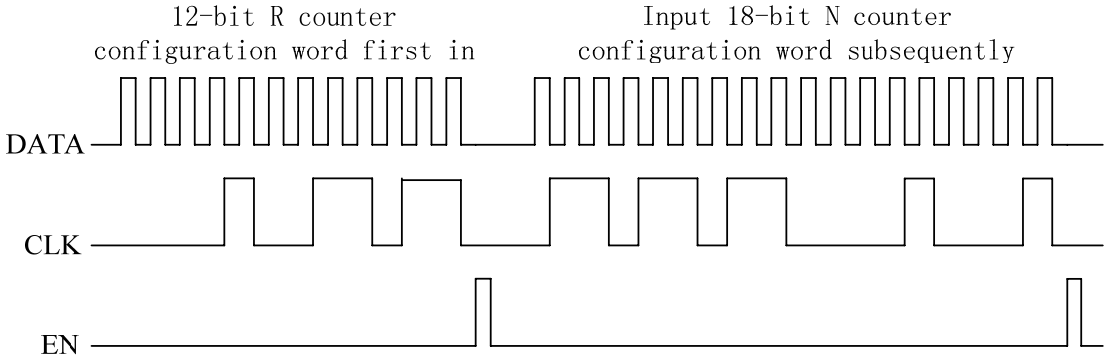
- Reference frequency 25 KHz (Example 1)
- Total number of frequency division 4× (16*B + A) = 863MHz÷25KHz = 34520
- 16*B+A=8630
- Binary (16bit) "0010000110110110"
- Group identification code of frequency divider N "10"
- Configuration word (18bit) "100010000110110110"

LSB (input to register first) → MSB

0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	0	1

3.4.4 Timing example

Based on the calculation of two examples in 3.4.3, only by inputting control word to MCU according to the following timing, PLL will be fixed at 863MHz. The timing of 3-line control end is as follows:



In ROM mode, it is unnecessary to calculate and set 3-line control timing. Only by setting logic level of 8 data ports D0-D7 as 00001111 according to TX frequency in *ROM Control Logic of D2009 Module*, reference frequency divider and channel frequency divider will set internally and automatically according to the above diagram, and PLL will be fixed at 863MHz.

3.5 864 MHz transceiving example by using the module

The first step: D2008TX adopts internal ROM distribution code. According to *ROM Control Logic of D2008 Module*, control logic of P phase is 1111-0110. Please set MODE pin as low level (ROM mode), and H/L as low level (high output power). The wiring mode is as Diagram 1.

The second step: D2008RXM adopts internal MCU. According to *ROM Control Logic of D2008 Module*, control logic of P phase is 1111-0110. And then match antenna, lead audio signal and RSSI signal. The wiring mode is as diagram 2.

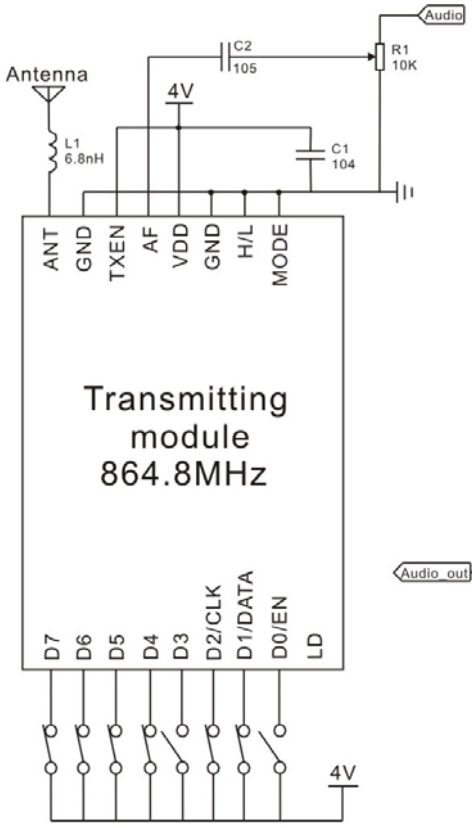


Figure 1 D2008TX（864.8MHz）

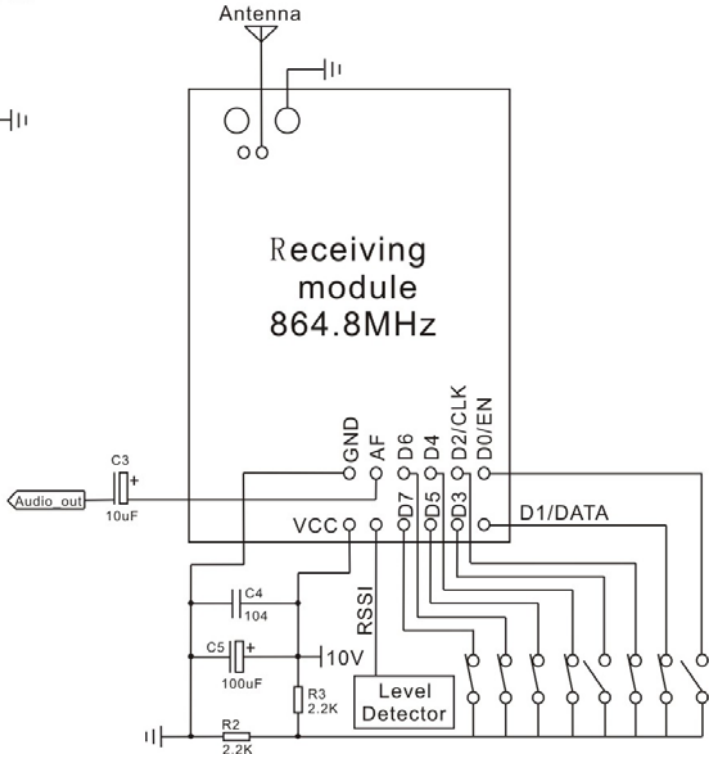


Figure 2 D2008RXR（864.8MHz）

4 FAQs

4.1 By using D2008 module, is only decimal accuracy possible for frequency?

A: If 25K is used as reference frequency, only decimal accuracy could be possible for fixed frequency. If 6.25K is used as reference frequency, accuracy of three figures after the decimal point could be possible for fixed frequency. The reference frequency ×4 is the accuracy of fixed frequency.

4.2 Is VCO bandwidth possible to exceed 30MHz?

A: Yes, the bandwidth is basically 10% of operating frequency. However, restricted by filter and modulation degree ±1.5KHz.it is hard to reach 10%.

4.3 The operating frequency of D2008 module is 300-1000MHz, does each module work within this range?

A: No, each module works within a certain bandwidth 30-90MHz in the range of 300-1000MHz.

4.4 Could the size of TX and RX module possible be changed according to customers' requirement?

A: Yes. There is no extra charge if circuit is not modified, only RF shape is enlarged. However, there is extra charge if size is to be reduced by re-designing RF circuit.

4.5 What is the wiring mode of module and wireless MIC main board?

A: TX module is usually welded on transmitting board. RX module is recommended to assemble separately instead of welding on receiver, in order to save PCB material.

4.6 What is the operating temperature range of the module?

A: The core chip works between -40°C and +85 °C. The operating temperature mainly depends on operating parameters with crystal oscillation. Ordinary 20M SMT crystal matching with the module works between -10 °C and +65 °C. If operating temperature range is to be expanded, general crystal should be replaced by temperature compensation crystal, and circuit design should be modified, which leads to extra charge.

4.7 Does MC Devices provide audio circuit module matching with RF module D2008?

A: MC Devices only provide the circuit design and products for some customers.

4.8 Please recommend operating voltage to generate lower phase noise.

A: Although RX may input voltage 10-16V, PLL chips in module is designed to be fixed at 4.5V to get the lowest phase noise. Therefore, it is OK that RX operating voltage is 10-16V. For TX, try to use high voltage, with the highest 4.5V.

4.9 How many frequencies are possible by using D2008 module?

A: 300. For details please refer to 3.1 and 3.3.

Important Notice

MC Devices reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to MC Devices' terms and conditions of sale supplied at the time of order acknowledgment.

MC Devices warrants performance of its products to the specifications applicable at the time of sale in accordance with MC Devices' standard warranty. Testing and other quality control techniques are also support this warrant.

美芯集成电路（深圳）有限公司
中国深圳高新区科技中二路软件园一期四栋 516 室

电话：（86）755-8618-5088
传真：（86）755-8618-5000
Email：sales@mcdevices.com
网址：www.mcdevices.com

MC DEVICES Co., Ltd

516 Bld. 4, National Software Park, 2 Kejizhong Rd.,
Shenzhen Hi-Tech Park,
Shenzhen, Guangdong, China
Tel: 86-755-8618-5088
Fax:86-755-8618-5000
Email: sales@mcdevices.com
http://www.mcdevices.com